IN THE CLAIMS:

(1) Please amend Claim 1 as follows:

1. (Amended) An integrated circuit comprising:

a substrate;

a plurality of bond pads formed above the substrate; and

a first isolated conductive trace formed at an outer region of the substrate and coupled to at least two of the plurality of bond pads.

(2) Please amend Claim 2 as follows:

2. (Amended) The integrated circuit of Claim 1 wherein the first isolated conductive trace surrounds a plurality of bond pads.

(3) Please amend Claim 3 as follows:

3. (Amended) The integrated circuit of Claim 2 wherein the first isolated conductive trace has a chamfered region.

(4) Please amend Claim 4 as follows:

4. (Amended) The integrated circuit of Claim 1 further comprising:

second conductive regions adapted to interconnect devices formed in the integrated circuit, wherein the first isolated conductive trace is separate from the devices.

(5) Please amend Claim 5 as follows:

5. (Amended) The integrated circuit of Claim 1 wherein the first isolated conductive trace comprises at least two separate first isolated conductive traces.

(6) Please amend Claim 6 as follows:

6. (Amended) The integrated circuit according to Claim 5 wherein the at least two separate first isolated conductive traces have a varying height relative to an upper surface of the substrate.

Cont. A1

(7) Please amend Claim 7 as follows:

7. (Amended) The integrated circuit according to Claim 1 wherein the first isolated conductive trace is formed at the periphery of the integrated circuit.

(8) Please amend Claim 8 as follows:

8. (Amended) The integrated circuit of Claim 1 wherein the first isolated conductive trace comprises at least two separate isolated conductive traces, each of the separate isolated conductive traces coupled to at least two of the plurality of bond pads.

(9) Please cancel Claim 9 without prejudice or disclaimer.

(10) Please amend Claim 10 as follows:

10. (Amended) An integrated circuit comprising:

Sub A2

a substrate;

a plurality of bond pads; and

an isolated conductive tester runner formed on the substrate and around the plurality of bond pads, the isolated conductive tester runner electrically coupled to at least two of the plurality of bond pads.

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[(11) Please amend Claim 11 as follows:]

11. (Amended) The integrated circuit of Claim 10 further comprising a plurality of isolated conductive tester runners.

[(12) Please amend Claim 12 as follows:]

12. (Amended) The integrated circuit according to Claim 11 wherein at least two of the plurality of the isolated conductive tester runners having a varying height relative to an upper surface of the substrate.

[(13) Please amend Claim 13 as follows:]

13. (Amended) The integrated circuit of Claim 10 wherein the isolated conductive tester runner has a chamfered region.

[(14) Please amend Claim 14 as follows:]

14. (Amended) The integrated circuit of Claim 10 further comprising:

devices formed on the integrated circuit; and

circuit conductive runners adapted to interconnect the devices to form a circuit;

wherein the isolated conductive tester runner formed on the substrate and around the plurality of bond pads is separate from the devices.